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RT8H062E

WATCH DOG TIMER

TERMINAL FUNCTION

Terminal No.	Symbol	Function
Undecided	VCC	Supply voltage terminal
	R	To change vcc detective voltage terminal
	WD	Watch dog input terminal
	C	To set abnormal high section of watch dog input terminal
	TC	To set watch dog time terminal
	Delay	To set power on reset time. Connection capacity terminal
	OUT	If input abnormal watch dog signal, then it output reset signal.
	GND	Ground terminal

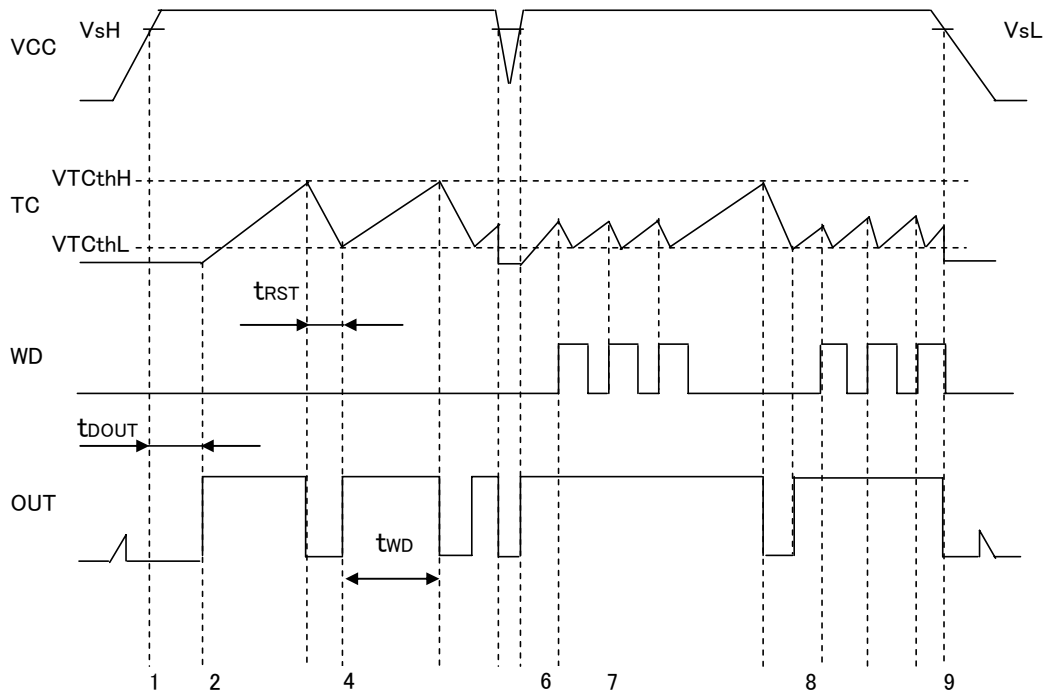
ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Symbol	Parameter	Ratings	Unit
VCC	Supply voltage	10	V
VIN	Input voltage (WD,C,TC,Delay)	-0.3~VCC	V
IOUT	Output current (OUT)	10	mA
Pd	Internal power dissipation	200	mW
Topr	Operating temperature	-20~+75	°C
Tstg	Storage temperature	-40~+150	°C

ELECTRICAL CHARACTERISTIC (Ta=25°C, VCC=3.3V unless otherwise noted.)

Symbol	Parameter	Test conditions	Designed value			Unit
			Min	Typ	Max	
ICC	Circuit current		360	600	840	μA
VsH	VCC detective voltage at High	OUT=VCC-100kΩ, OUT:L→H	2.73	2.87	3.01	V
VsL	VCC detective voltage at Low	OUT=VCC-100kΩ, OUT:H→L	2.62	2.76	2.90	V
VWDth	Threshold voltage of WD	C:L→H		1.3		V
IWD	WD input current	WD=3V	80	160	320	μA
IC	Output current C	WD=3V, C=0.3V		20		μA
VTCthH	Threshold voltage of TC HIGH	OUT=VCC-100kΩ, OUT:H→L		1.5		V
VTCthL	Threshold voltage of TC LOW	OUT=VCC-100kΩ, OUT:L→H		1.1		V
VDth	Threshold voltage of Delay	OUT=VCC-100kΩ, OUT:L→H		1.2		V
IDelay	Charge current of Delay	Delay=0V		5		μA
VOsat1	OUT saturation voltage1	VCC=1.2V, I=1mA		0.12	0.50	V
VOsat2	OUT saturation voltage2	VCC=3V, TC=3V, I=1mA		0.10	0.50	V

TIMING DIAGRAM



NOTES

1. The VCC rises up to detective voltage(VsH), then reset is released.
2. OUT terminal(Open collector) generate High signal, after tDOUT time decided from capacity at Delay terminal.
Charge of TC begins.
 $t_{DOUT}[s] \approx C_{delay}[F] \times 1.2[V] \div 5E-6[A]$
3. This MFT watch WD signal from when TC rises up from VTcThL to VTcTh. If no signal input WD, OUT terminal generate Low signal.
 $t_{WD}[s] \approx 0.236 \times C_{TC}[F] \times R[\Omega]$
4. When TC falls to VTcThL, OUT terminal generate High signal.
 $t_{RST}[s] \approx 100 \times C_{TC}[F]$
5. Due to the power failure etc, VCC falls to VsL, OUT terminal generate Low signal.
6. VCC rises up to VsH, OUT terminal generate High signal (if no Cdelay capacity).
7. If normal clock signal is entered in twd time, TC terminal is discharged. And if TC terminal falls to VTcThL, TC begins charge.
8. If no signal is entered in twd time, OUT terminal generate Low signal.
9. When VCC falls to VsL, OUT terminal generate Low signal.

***About C terminal**

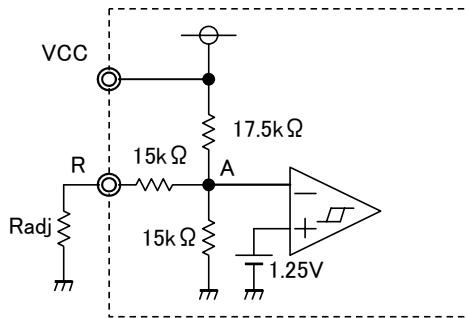
Please connect capacity C terminal-GND terminal always. This capacity is always necessary for detected edge of WD signal
And, for detected abnormal state of WD's high fixation, This capacity can detect normal time of WD's high fixation.

$$t_{wdh}[s] \approx 30000 \times C_c[F]$$

When High signal is entered in WD terminal, twdh[s] or more, TC terminal begins charge, and begin operate 3. .

About VCC detective voltage (R terminal)

VCC detective voltage	At Open	At 3.3kΩ pull down
VsH	2.87V	4.15V
VsL	2.76V	3.98V

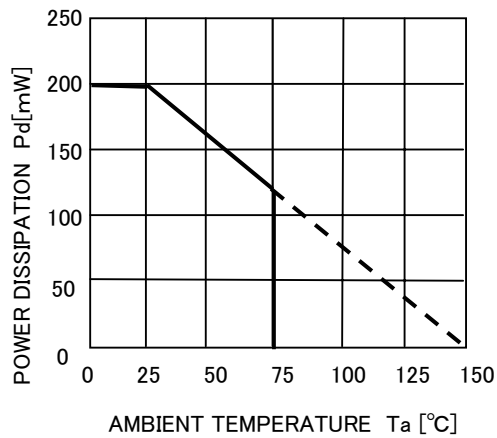


If change Radj, VCC detective voltage is variable.

$$VsH \doteq (1 + 17.5k / \text{Combined resistance between point A} \sim \text{GND}) \times 1.32V$$

$$VsL \doteq (1 + 17.5k / \text{Combined resistance between point A} \sim \text{GND}) \times 1.25V$$

THERMAL DERATING





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